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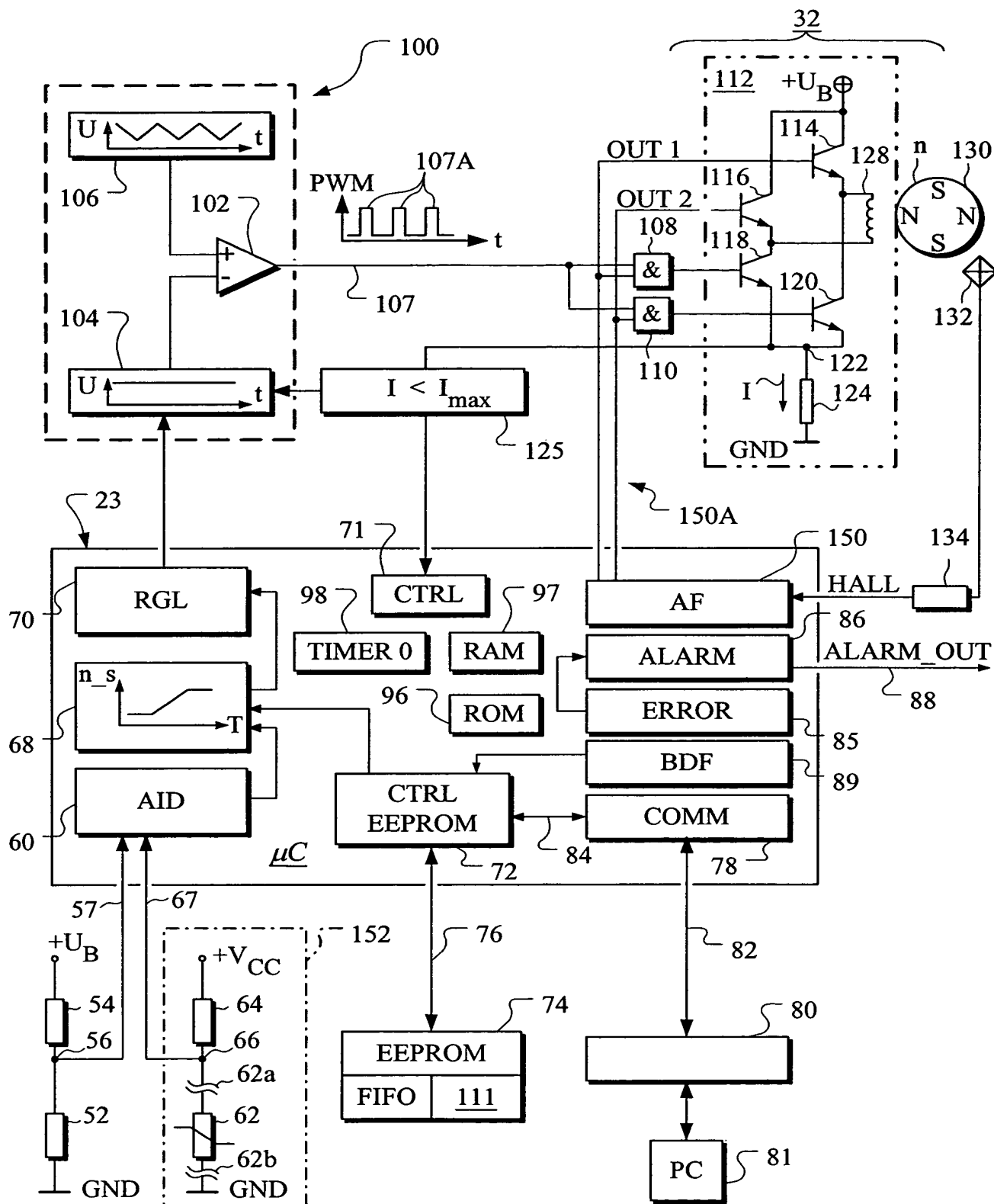


Fig. 2

Fig. 3

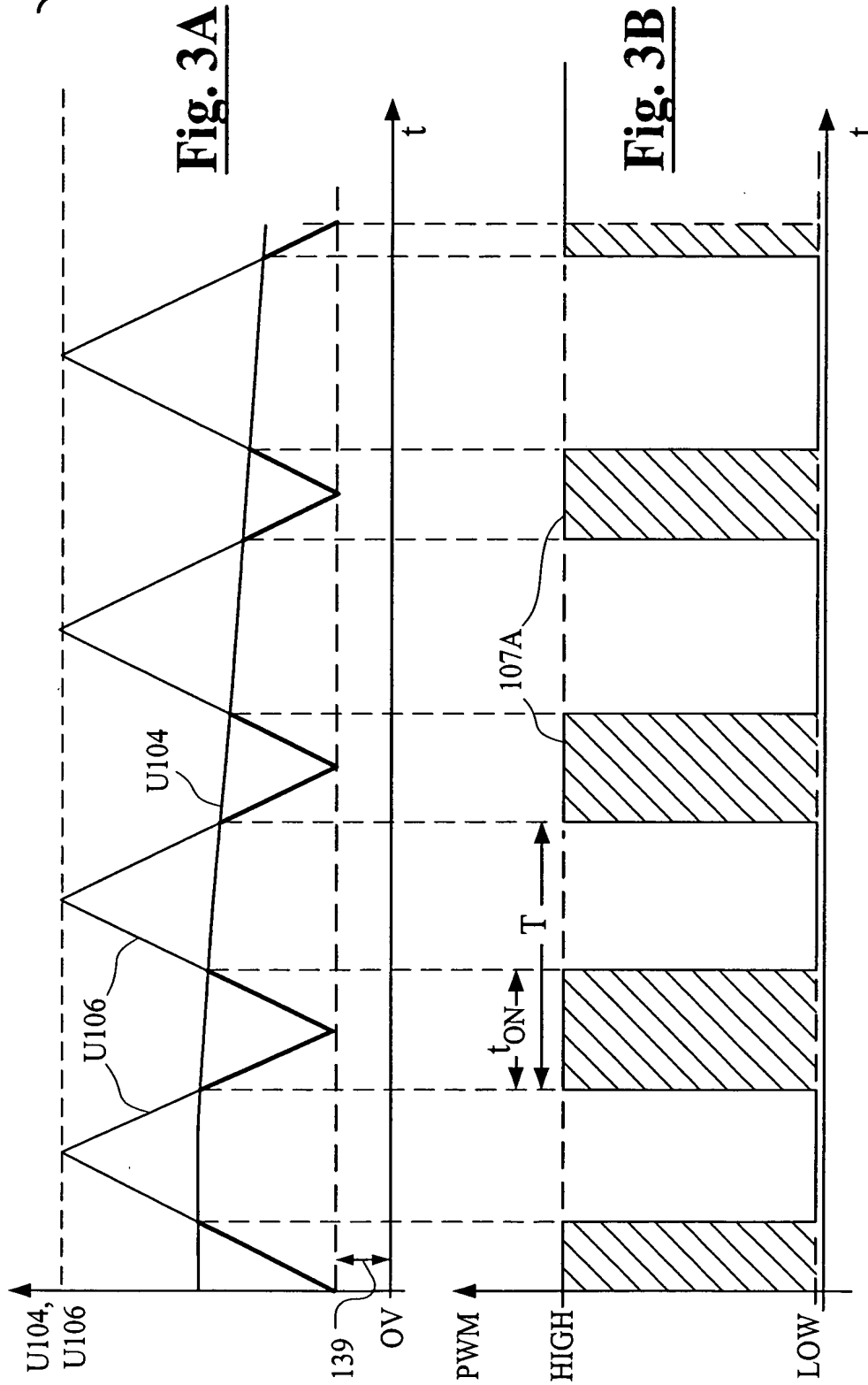


Fig. 3A

Fig. 3B

Fig. 3C

$$\text{PWM_TV} = \frac{t_{\text{ON}}}{T}$$

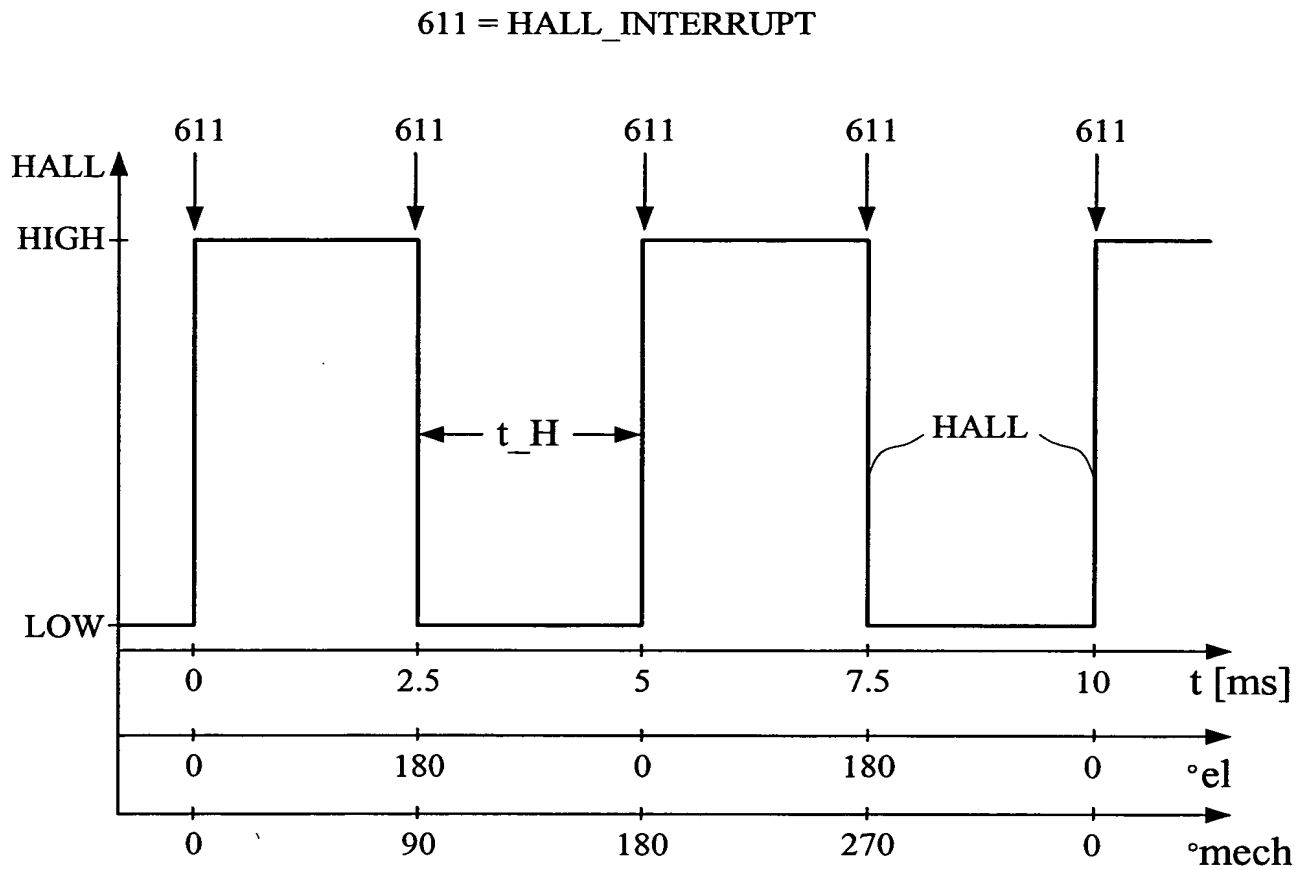


Fig. 4

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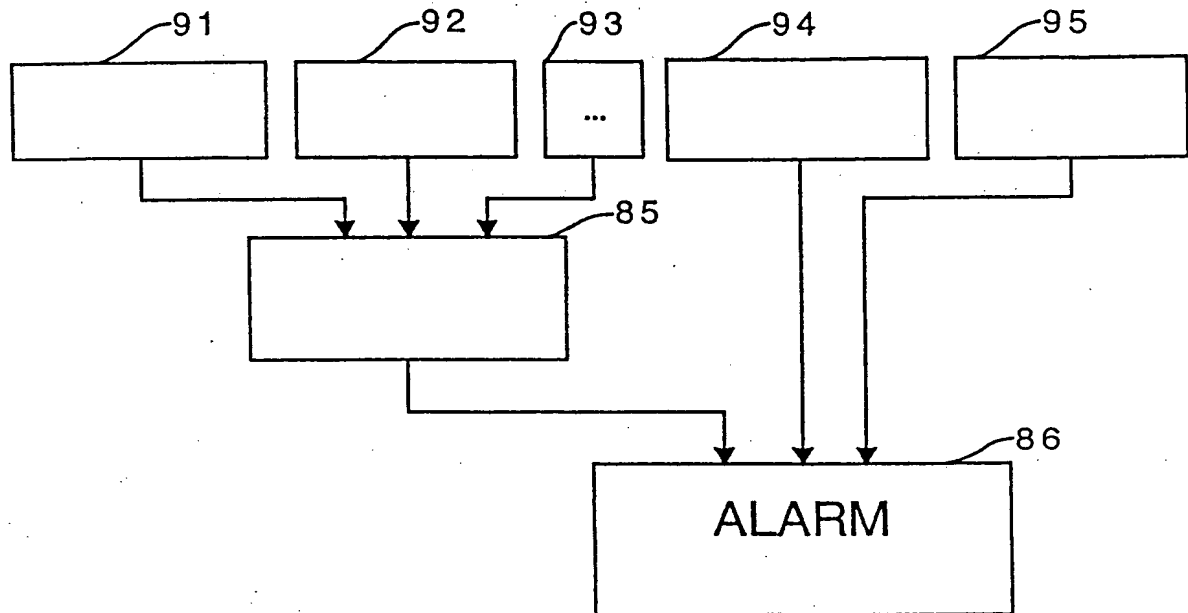


Fig. 5

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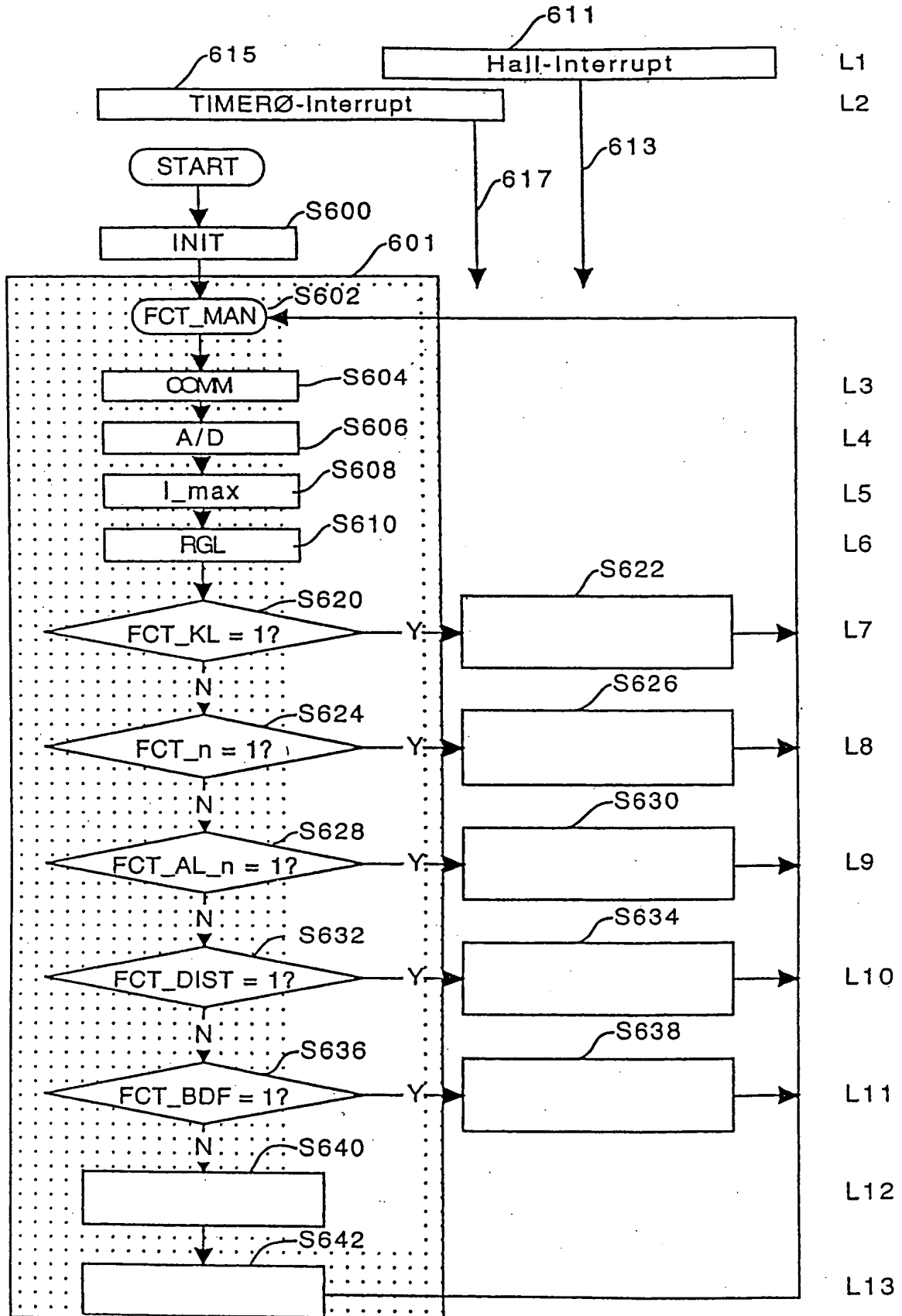


Fig. 6

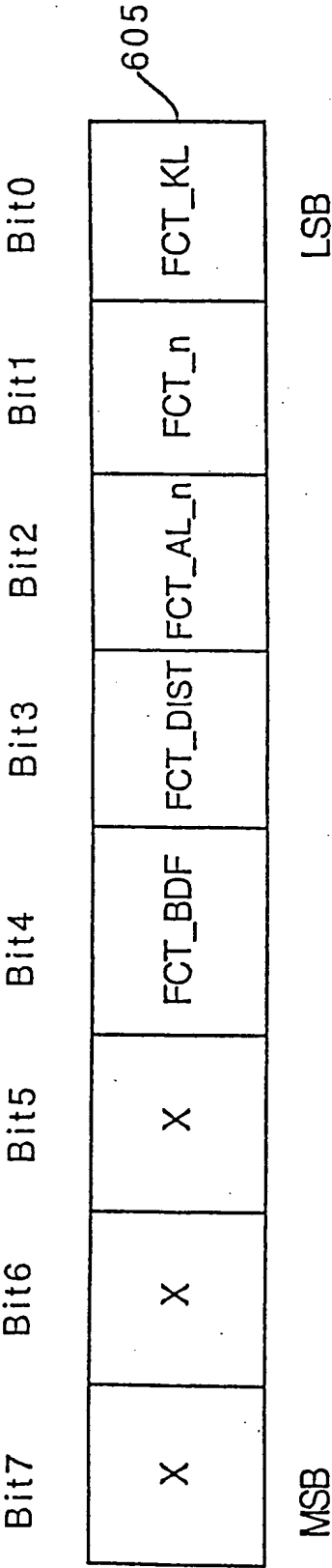


Fig. 7

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Objecttable

Index	Memorytype	Access	Name
0x20	unsigned8	RW	DIST_CTRL
0x21	unsigned8	RW	DIST_STATE
0x22	unsigned16	RW	DIST_CODE
0x23	unsigned8	RW	DIST_REAC
0x24	unsigned8	RW	n_DIST
0x25	unsigned8	RW	t_COMM_TO
0x30	unsigned8	RW	OD_TMAX
0x31	unsigned8	RW	OD_UBMAX
0x32	unsigned24	RW	OD_OHO
0x33	unsigned24	RW	OD_COMMUT

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Fig. 8

DI_CTRL

Bit	Name	LOW	HIGH
0	DC_LATCH	NO_LATCH	LATCH
1-6	RES		
7	DC_CLEAR	0 -> 1 -> 0 to clear	

Fig. 9

DI_STATE

Bit	Name	VAL	Meaning
0-2	DS_CLASS	0	DS_μC
		1	DS_COMM
		2	DS_SENS
		3	DS_HW
		4-7	RES
3-6	RES		
7	DS_ACTIVE	0	NO_DIST
		1	DIST

Fig. 10

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DI_CODE (16 Bit)

Class	VAL	Name
DS_μC	0-999	
	0	DN_WDT
	1	DN_CHKS_ROM
	2	DN_CHKS_RAM
	3	DN_CHKS_EEPROM
	4	DN_TEST_RAM
	5-999	RES
DS_COMM	1000-1999	
	1000	DN_TIMEOUT_TRANSFER
	1001	DN_TIMEOUT_BUS
	1002	DN_PROT_ERR
	1003	DN_INVAL_DATA
	1004-1999	RES
DS_SENSOR	2000-2999	
	2000	DN_SENSOR_INTERRUPT
	2001	DN_SENSOR_SHORT
	2002-2999	RES
DS_HW	3000-3999	
	3000	DN_DRIVER_FAULT
	3001-3999	RES
RES	4000-65535	

Fig. 11

DI_REAC

Bit	Name	VAL	Meaning
0-2	DR_REAC	0	DR_OFF
		1	DR_n_max
		2	DR_n_min
		3	DR_n_0
		4	DR_n_DIST
		5	DR_BRAKE
		6-7	RES
3	DR_AL	0	DR_AL_OFF
		1	DR_AL_ON
4-7	RES		

Fig. 12

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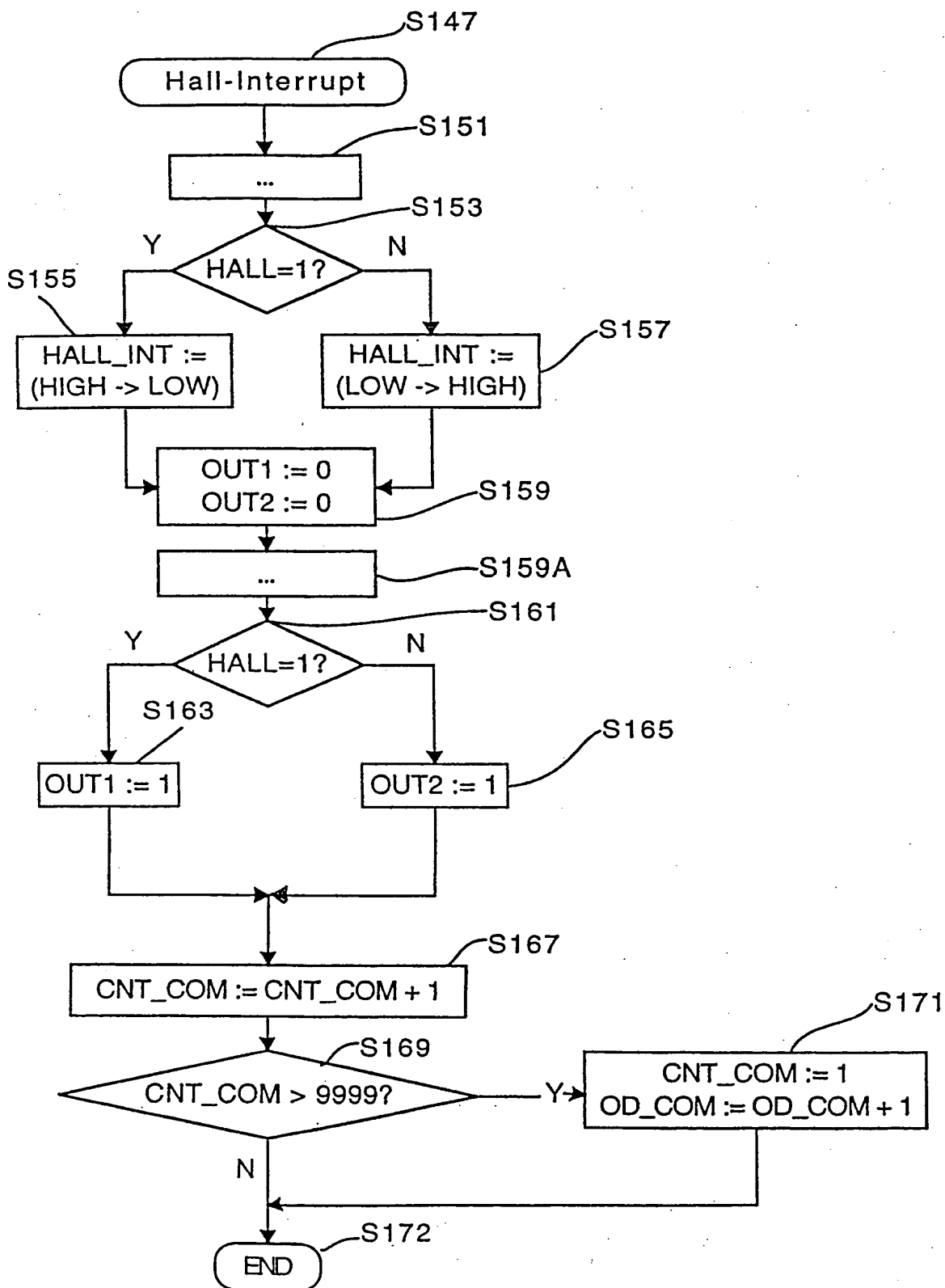


Fig. 13

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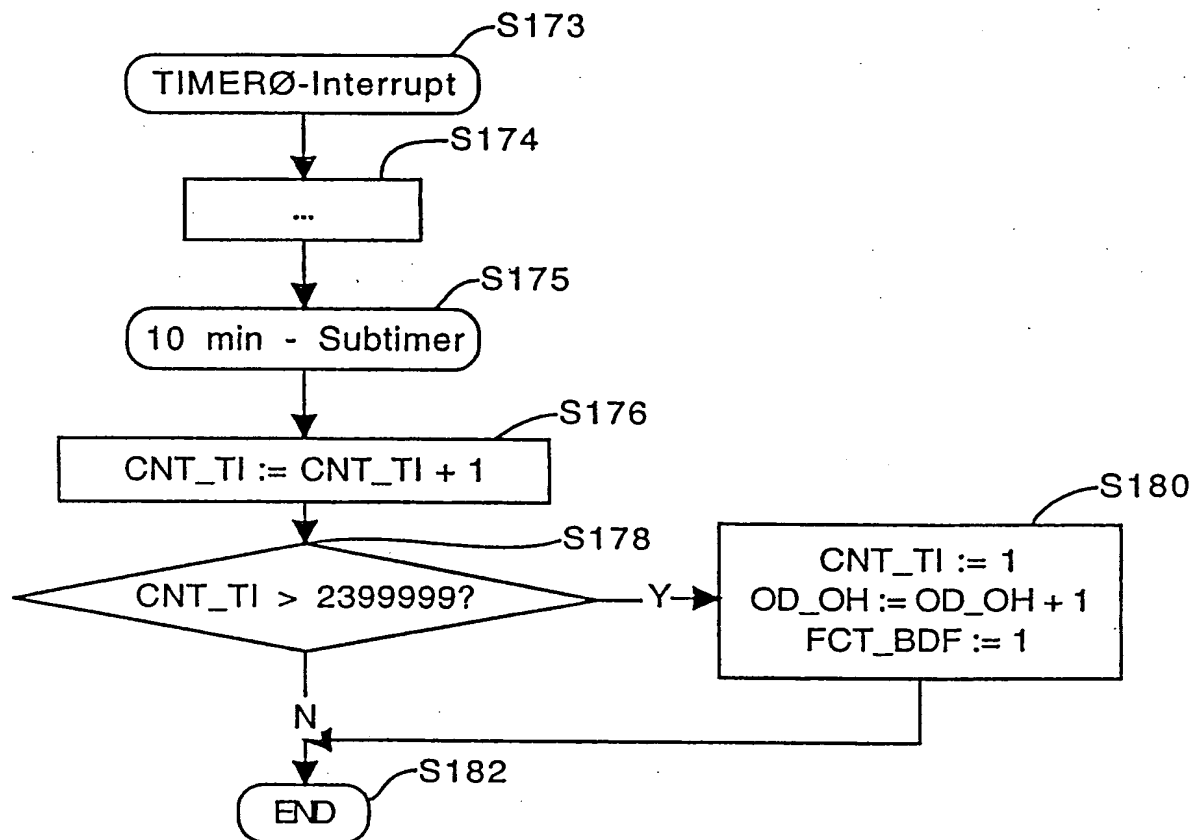


Fig. 14

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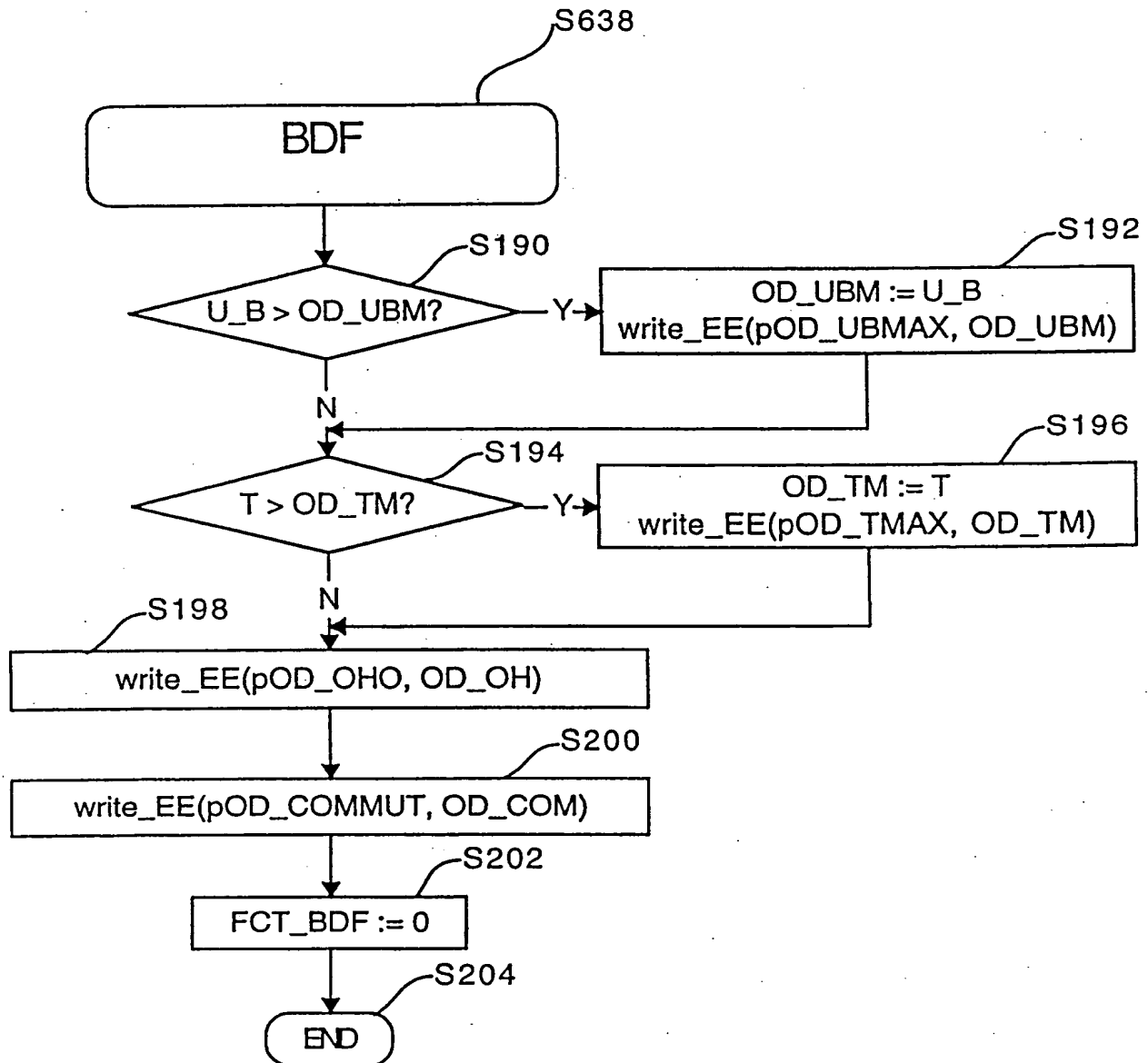


Fig. 15

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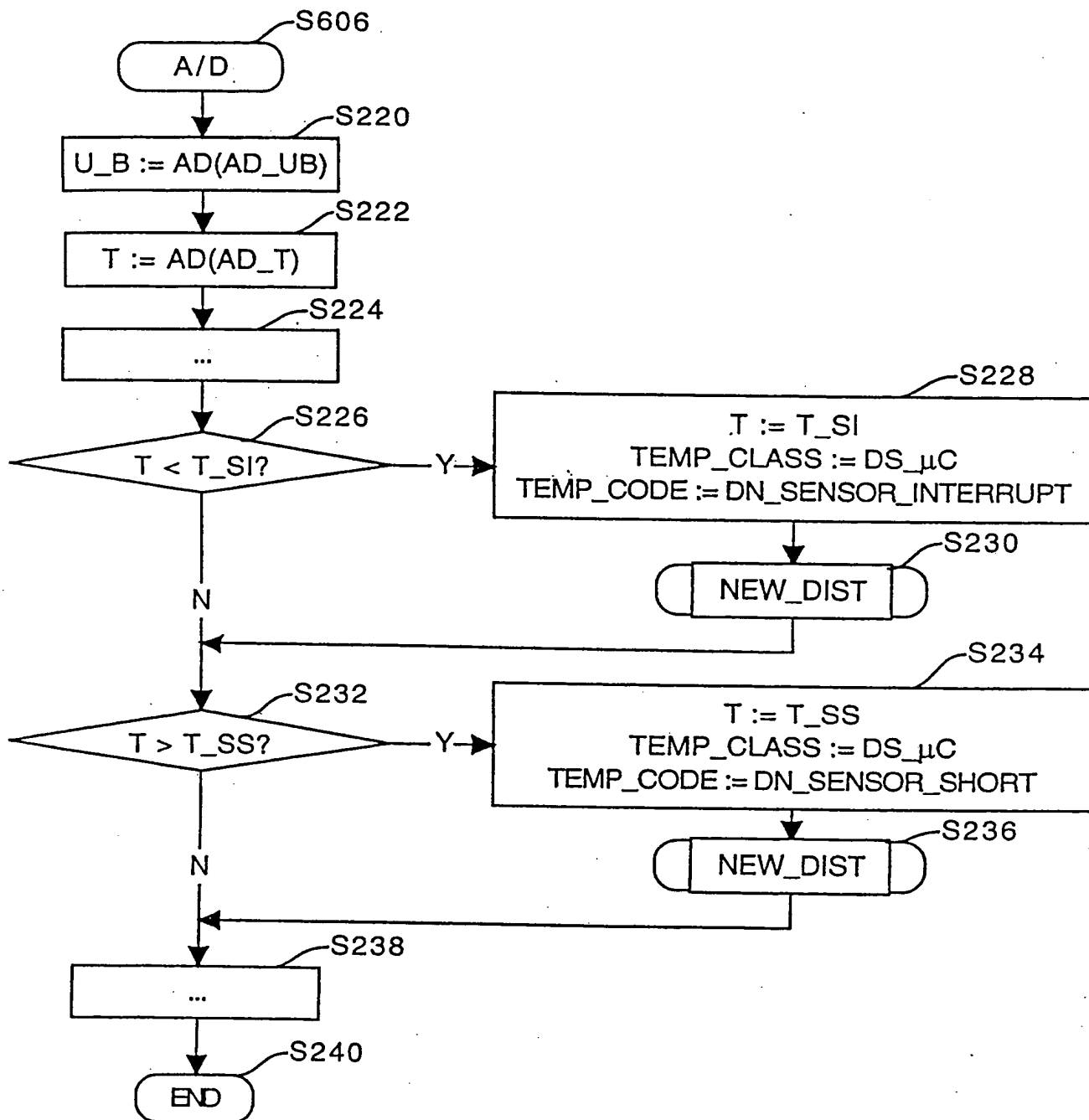


Fig. 16

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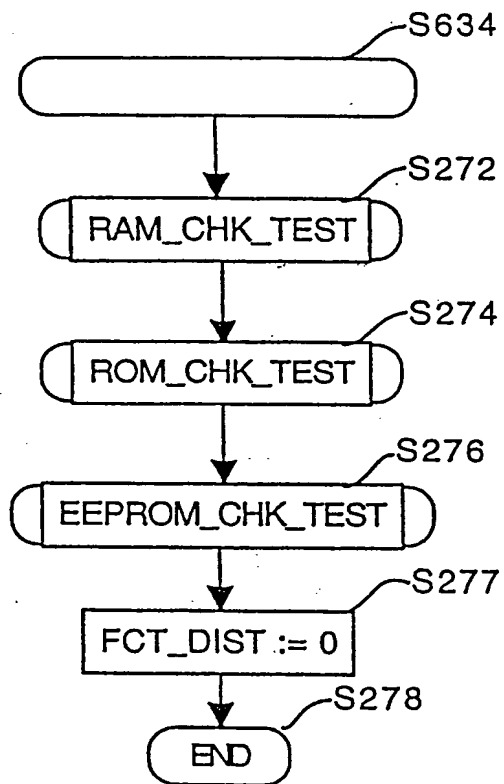


Fig. 17

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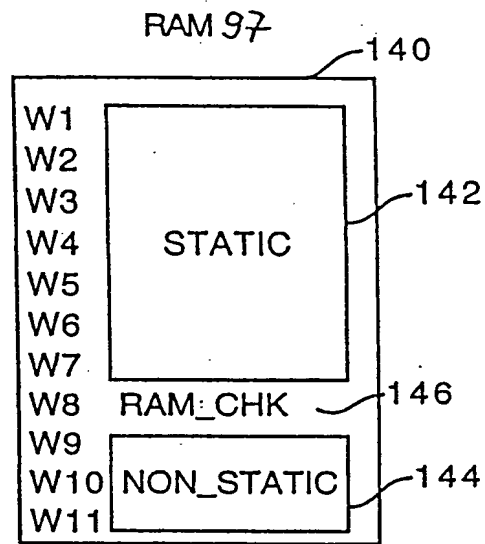


Fig. 18

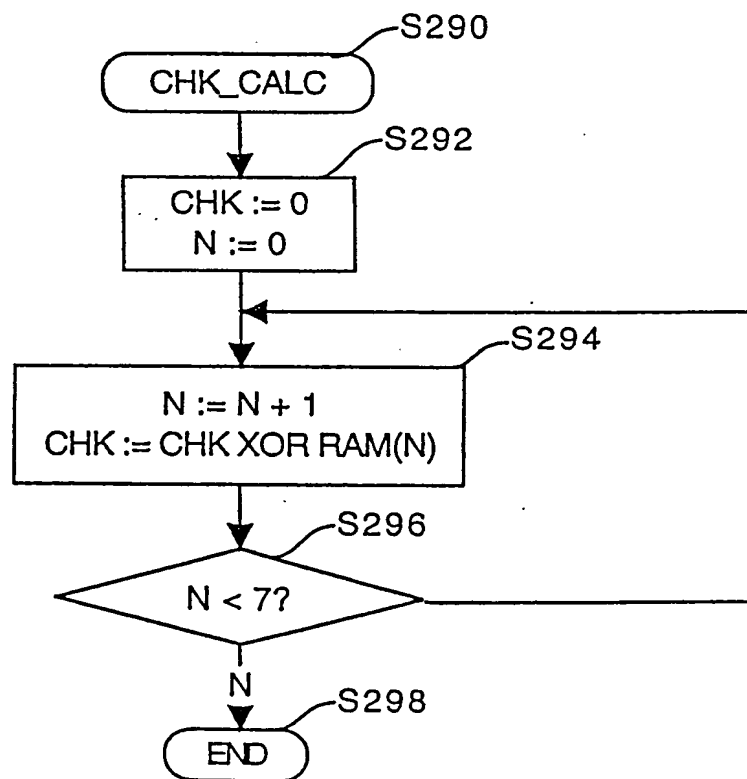


Fig. 19

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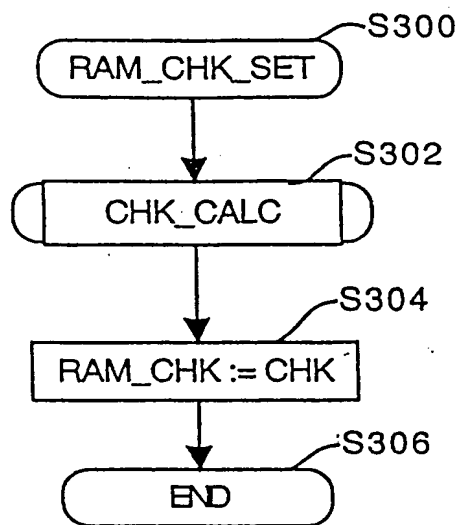


Fig. 20

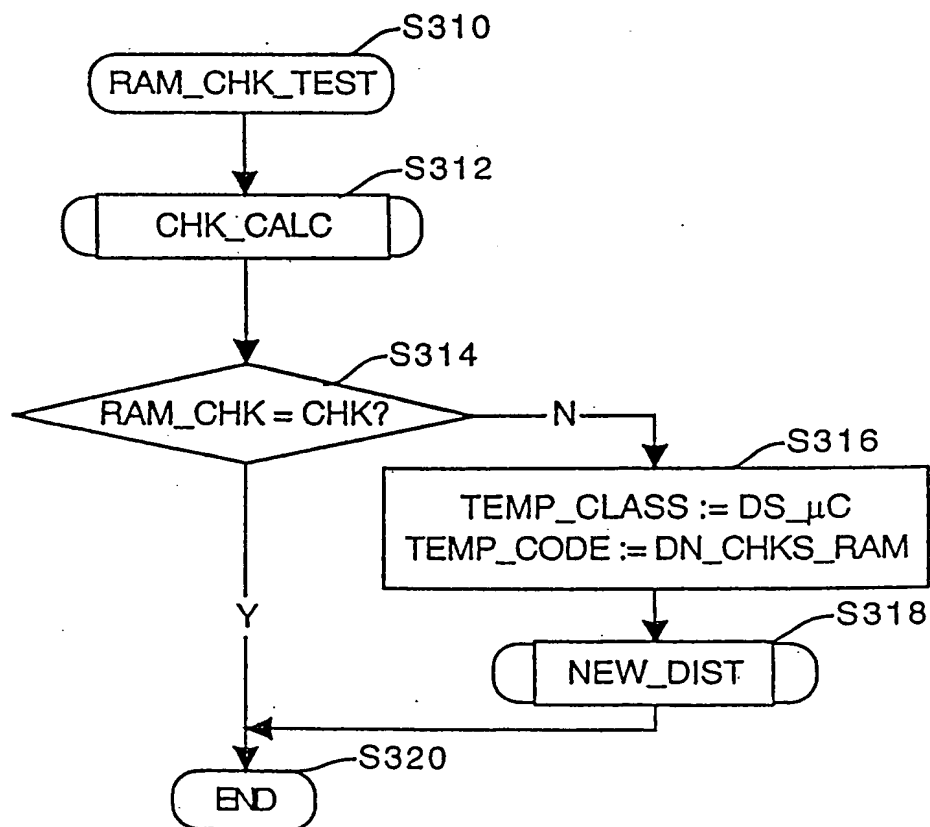


Fig. 21

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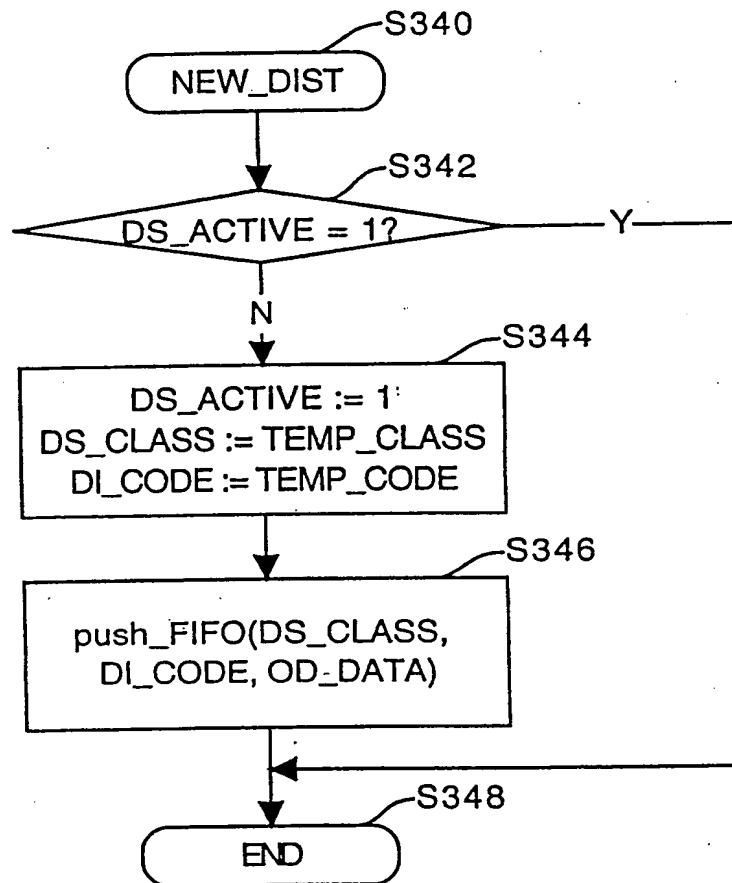


Fig. 22

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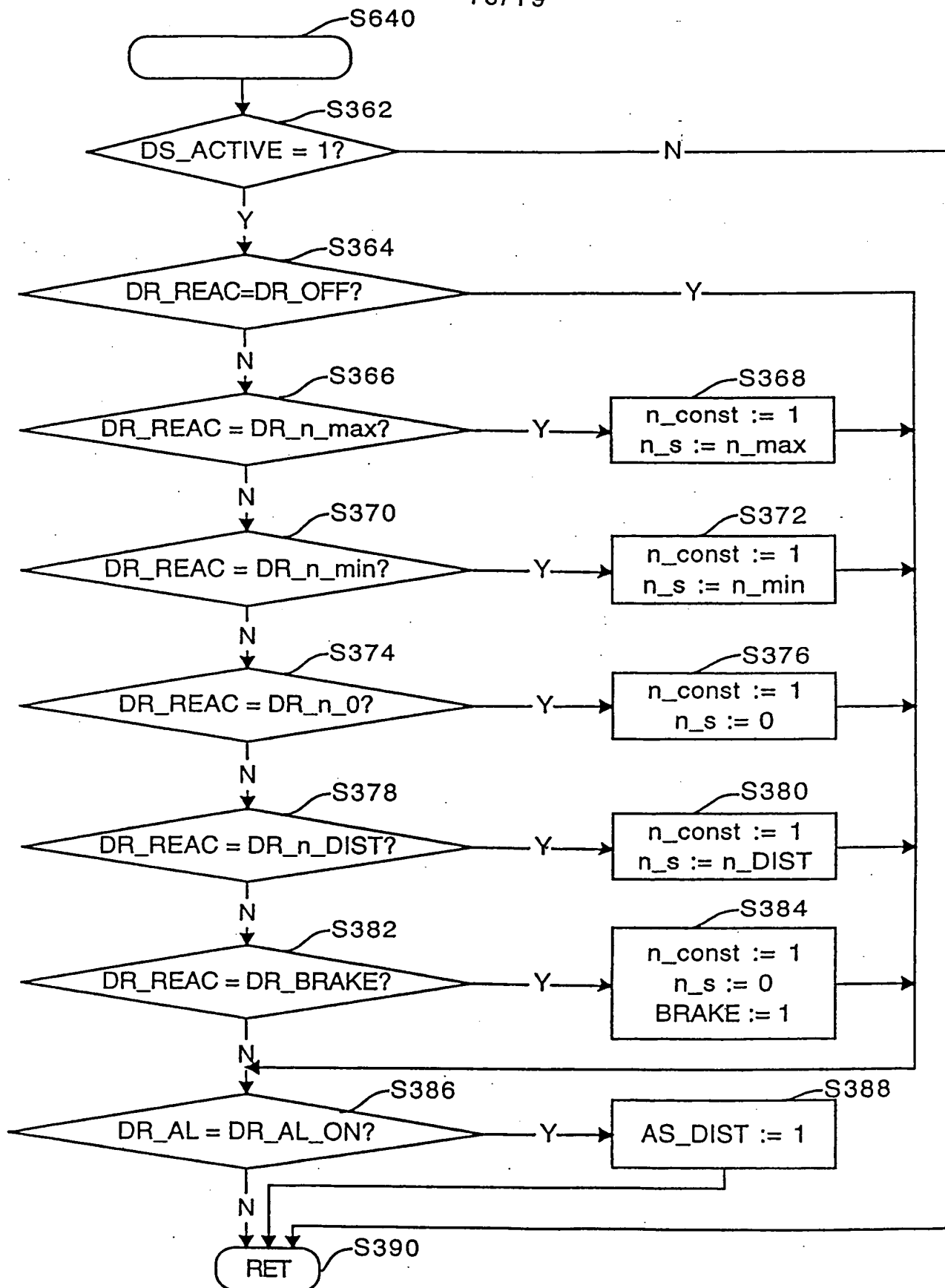


Fig. 23

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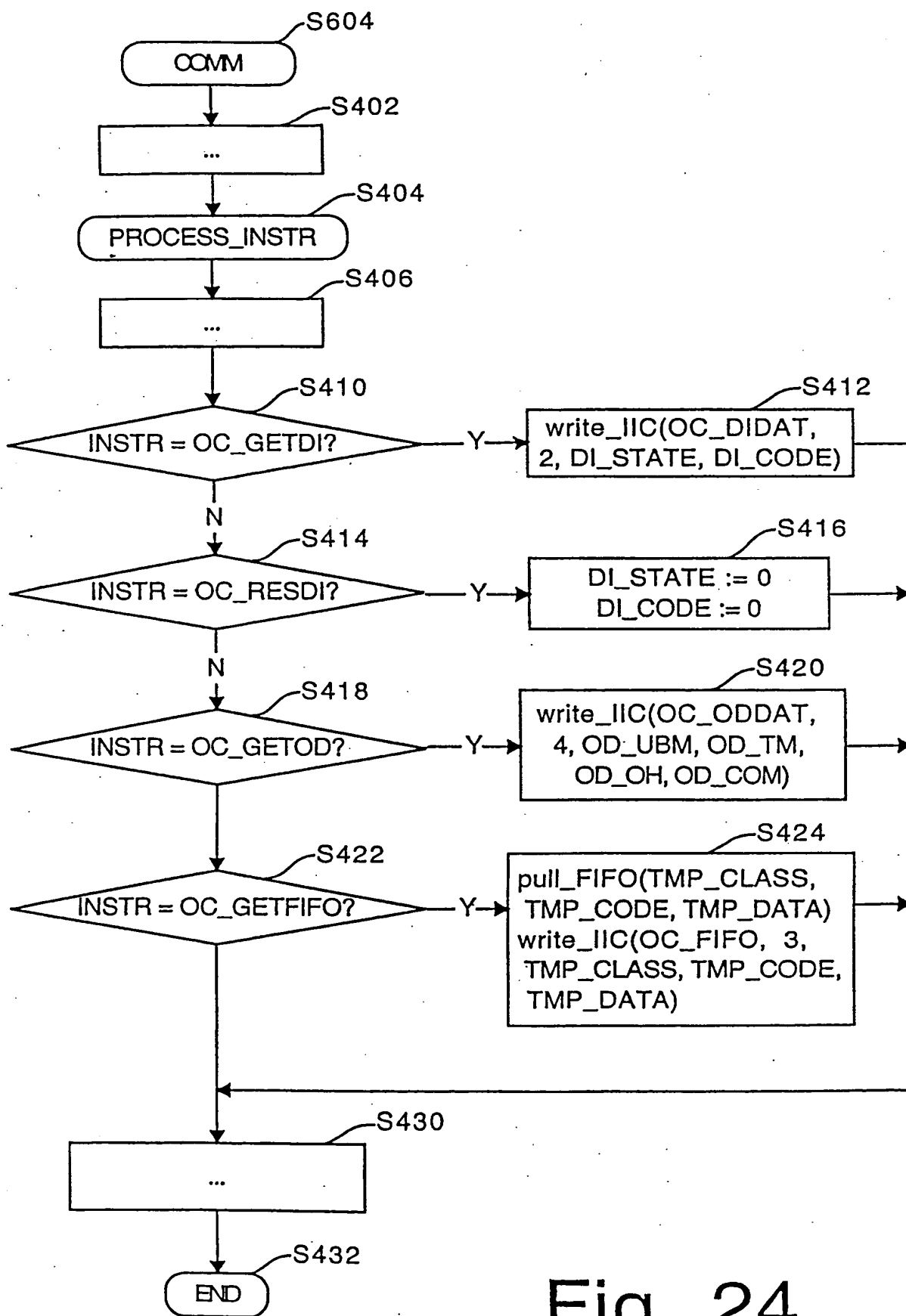


Fig. 24